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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,524	11/25/2003	Kai-Chiang Wu	MR1035-1345	5153

4586 7590 10/17/2005

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,524	WU, KAI-CHIANG	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/720524 Attorney's Docket #: MR1035-134
Filing Date: 11/25/2003;

Applicant: Wu

Examiner: Alexander Williams

Applicant's election of Group I (claims 1 to 3), filed 9/27/05, has been acknowledged.

Claims 4 and 5 have been cancelled.

Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that

the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 3 are rejected under 35 U.S.C. § 102(e) as being anticipated by Liu et al. (U.S. Patent # 6,919,627 B2).

1. Liu et al. (figures 1 to 7) specifically figure 1 show a chip adhesive **13** adhered to a stacked packaging structure **1** between two adjacent chips **11,14**, and the chip adhesive includes a plurality of stuff particles **131** to keep the chip adhesive with a predetermined thickness.

2. The chip adhesive of claim 1, Liu et al. can further control the thickness through suitably selecting a type of the stuff particle.

3. The chip adhesive of claim 1, Liu et al. can further control the thickness through suitably selecting a quantity of the stuff particle.

ABSTRACT:

A multi-chip module is proposed, which is designed to pack two or more semiconductor chips in a stacked manner over a chip carrier in a single package. The multi-chip module is characterized by the use of adhesive with fillers to allow the topmost chip (i.e. the second chip) superimposed to the bottommost chip (i.e. the first chip) after the first chip electrically connected to the chip carrier. The thickness of the adhesive layer depends on the diameter of the fillers higher than loop height of the bonding wires that is positioned above the active surface of the first chip to prevent the bonding wires connected to the first chip to come in contact with the overlaid chip. Alternatively, stacked chips formed via the adhesive layer can take shorter processing time to be reduced cost and simplify processes than working procedures in the prior art. Moreover, the other embodiment of the fillers (such as copper or aluminum) with high thermal conductivity is also capable of enhancing heat dissipation of the stacked package application.

[0011] According to the above and other objectives, a multichip module is proposed, comprising: a chip carrier; at least one first chip having an active surface and an opposing non-active surface, allowing the first chip to be adhered to the chip carrier via the non-active surface; a plurality of first bonding wires which one end thereof is bonded to the active surface of the first chip and the other end is bonded to the chip carrier for providing electrical connection between the first chip and the chip carrier; at least one second chip having an active surface and an opposing non-active surface; an adhesive layer applied over the active surface of the first chip, containing a plurality of fillers therein in which the diameter of the fillers determines the thickness of the adhesive layer which is made just higher than the loop height of the bonding wires after adhering the second chip to the first chip

via the non-active surface of the second chip; a plurality of second bonding wires for providing electrical connection between the second chip and the chip carrier; and an encapsulant for encapsulating the first chip, the first bonding wires, the second chip and the second bonding wires.

[0012] A manufacturing method of the multichip module is proposed, comprising the steps as follows: firstly, adhering at least one first chip having an active surface and a non-active surface to a chip carrier; then using a plurality of first bonding wires to electrically connect the active surface of the first chip to the chip carrier; following that, applying an adhesive over the active surface of the first chip, in which the adhesive contains a plurality of fillers having a predetermined diameter for determining the thickness of the adhesive; then adhering at least one second chip to the first chip via the adhesive, in which the adhesive layer formed between the first chip and the second chip must be larger than the loop height of the first bonding wires; After that, using a plurality of second bonding wires to electrically connect the second chip to the chip carrier. This is then followed by a molding process and other latter procedures.

[0013] In another embodiment of the present invention, a third chip is further adhered onto the second chip to form a stacked multichip module with three chips perpendicularly mounted on top of the other. Because the diameter of the fillers contained in the adhesive is larger than the loop height, the size of the third chip is not restricted as contact made between the third chip and the gold wires is prohibited, allowing more same sized chips to be received in a same semiconductor package.

[0014] Yet, in another embodiment of the present invention is disclosed, reverse bonding technique is utilized to substantially reduce the loop height of the first bonding wires, allowing fillers with smaller diameters to be used, so as to reduce the thickness of the adhesive, and thereby achieving the objective of reducing the overall height of a semiconductor package.

[0015] The present invention solve those drawbacks from the prior arts by mixing a plurality of fillers into a dielectric or conductive adhesive and the diameter of the filler determines the thickness of the adhesive layer between the topmost and bottommost chip. Fillers with an appropriate diameter are

chosen depending on the loop height of the first bonding wires (i.e. the distance between the active surface of the chip and the vertexes of the outwardly projecting loops of the bonding wires). When using conventional wire bonding technique, the loop height is high (approx. 4 mils) therefore fillers with larger diameter should be chosen, while when using reverse bonding technique, the loop height is low (approx. 2 mils) therefore filler with smaller diameter should be chosen. However the diameter of the fillers must be smaller than the loop height of the first bonding wires, so as to prevent contact between the second chip and the first bonding wires causing shortage.

[0041] Then, referring to FIG. 3E a chip bonding process is followed, allowing the second chip 14 to be pressed against the adhesive 13 via the non-active surface 141 itself. Since the diameter of the fillers 131 in the adhesive 13 is larger than the loop height of the first bonding wires 12, when a machine (not shown) is implemented for firmly pressing the second chip 14 against the adhesive layer 13, bond force for the chip is not required to be accurately controlled as inappropriate electrical connection between the second chip 15 and the first bonding wires 12 is prohibited, and as a result the manufacturing time and costs can be effectively reduced.

Claims 1 to 3 are rejected under 35 U.S.C. § 102(e) as being anticipated by Ismail et al. (U.S. Patent Application Publication # 2003/01060311 A1).

1. Ismail et al. (figures 3) show a chip adhesive **118** adhered to a stacked packaging structure **100** between two adjacent chips **104,106**, and the chip adhesive includes a plurality of stuff particles **120** to keep the chip adhesive with a predetermined thickness.

2. The chip adhesive of claim 1, Ismail et al. can further control the thickness through suitably selecting a type of the stuff particle.

3. The chip adhesive of claim 1, Ismail et al. can further control the thickness through suitably selecting a quantity of the stuff particle.

[0033] In accordance with the present invention, the adhesive material 118 includes a plurality of particles 120 blended

therein in order to maintain a predetermined spacing between the bottom die 104 and the top die 106 so that the wirebonds of the wires 122 are not damaged when the top die 106 is attached to the bottom die 104. The adhesive material 118 preferably comprises any of the typical adhesives used to attach one die to another die, so long as it is filled with particles sufficient to provide the aforementioned predetermined spacing. Typical adhesives are epoxy, cyanate ester and polyimide.

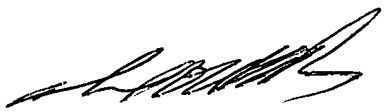
The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/777,686,685,723,728,724,725,784,786,787,788,789,790,795,783 428/323,402.24,402 156/273.7,312 174/88 R,868, 94 R	10/11/05
Other Documentation: foreign patents and literature in 257/777,686,685,723,728,724,725,784,786,787,788,789,790,795,783 428/323,402.24,402 156/273.7,312 174/88 R,868, 94 R	10/11/05
Electronic data base(s): U.S. Patents EAST	10/11/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
10/12/05